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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,727	06/26/2001	Daniel M. Kinzer	IR-1698 (2-2027)	1370

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EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 07/31/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/891,727	KINZER ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to the application filed June 26, 2001.

Information Disclosure Statement

2. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: a) 5 (See Figure 4); b) 4 (See Figure 5); c) 10 (See Figure 9); and d) 12 (See Figure 11). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "60" has been used to designate both drain and sinker (See Page 5 Paragraph 21 and Paragraph 25). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-6 and 8-21 are rejected under 35 U.S.C. 103(a) as obvious over Kitamura et al. (U.S. Patent No. 5,844,275) in view of Ranjan (U.S. Patent No. 5,861,657) and Sakakibara et al. (U.S. Patent No. 5,449,946).

In regards to claim 1, Kitamura et al. ("Kitamura") discloses the following:

a) a substrate (1) of one of the conductivity types (See Figure 1);

b) an epitaxially deposited trench receiving layer (2) of said one of the conductivity types supported atop said substrate and having an upper surface (See Figure 1);

c) a plurality of spaced laterally extending trenches formed into said trench-receiving layer (See Figure 9);

d) a diffusion of the other of said conductivity types extending into the walls of said trenches (3) and having a given depth and a given concentration (See Figure 1);

e) trenches defining mesas between them of a given width and a given concentration (See Figure 9);

f) a drain region (11) of said other of said conductivity types extending into, said trench receiving layer and disposed at the end of said mesas (See Figure 1); and

g) a MOSgate structure including a source region (9), base region (8) and a gate electrode (7) disposed at the other end of said mesas (See Figure 1).

In regards to claim 1, Kitamura fails to disclose the following:

a) a monocrystalline semiconductor wafer.

However, Sakakibara et al. ("Sakakibara") discloses a monocrystalline semiconductor wafer (See Column 1 Lines 59-62). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kitamura to include a monocrystalline semiconductor wafer as disclosed in Sakakibara because it aids in preventing capacitive coupling prevention.

b) the thickness and concentration of said mesas and said diffusions being selected to cause each to fully deplete under blocking voltage conditions.

However, Ranjan discloses a semiconductor device where the mesas and diffusions vary (See Column 2 Lines 7-16). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kitamura to include mesas and diffusions that vary as disclosed in Ranjan because it provides a smaller lateral extent and takes up less chip area.

In regards to claim 2, Kitamura discloses the following:

a) a dielectric filler (5) in each of said trenches (See Figure 1).

In regards to claim 3, Kitamura discloses the following:

a) source, drain and gate contacts (14, 7, and 15) supported on said upper surface and connected to said source region, gate electrode and drain regions respectively (See Figure 1).

In regards to claim 4, Kitamura discloses the following:

a) substrate is a lightly doped P type material (See Figure 1).

In regards to claim 4, Kitamura fails to disclose the following:

a) diffusion and said mesas have RESURF concentrations.

However, Ranjan discloses a semiconductor device where the mesas and diffusions have RESURF (See Column 1 Lines 17-20 and Column 2 Lines 7-16). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kitamura to include mesas and diffusions that have RESURF as disclosed in Ranjan because it aids in controlling the breakdown voltage.

In regards to claim 5, Kitamura fails to disclose the following:

a) a further region of said other conductivity interposed between said substrate and said trench receiving layer being more lightly doped than said diffusion.

However, Sakakibara discloses a further region (2a) of said other conductivity interposed between said substrate and said trench receiving layer (See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kitamura to include a further region as disclosed in Sakakibara because it aids in preventing capacitive coupling prevention.

b) diffusion extending into said further region along the bottoms of said trenches.

However, Ranjan discloses a semiconductor device where the diffusion (23) extends (See Column 2 Lines 7-16). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kitamura to include diffusion that extends as disclosed in Ranjan because it aids in the formation of isolated regions.

In regards to claim 6, Kitamura fails to disclose the following:

a) diffusion extending into said further region along the bottoms of said trenches.

However, Ranjan discloses a semiconductor device where the diffusion extends (See Column 2 Lines 7-16). It would have been obvious to one having ordinary skill in the art at the

time the invention was made to modify the semiconductor device of Kitamura to include diffusion that extends as disclosed in Ranjan because it aids in the formation of isolated regions.

In regards to claims 8 and 15, Kitamura discloses the following:

a) a dielectric filler in each of said trenches (See Figure 1).

In regards to claims 9, 11, 16 and 18, Kitamura discloses the following:

a) source, drain and gate contacts supported on said upper surface and connected to said source region, gate electrode and drain regions respectively (See Figure 1).

In regards to claims 10, 12-14, 17 and 19-21, Kitamura discloses the following:

a) substrate is a lightly doped P type material (See Figure 1).

In regards to claims 10, 12-14, 17 and 19-21, Kitamura fails to disclose the following:

a) diffusion and said mesas have RESURF concentrations.

However, Ranjan discloses a semiconductor device where the mesas and diffusions have RESURF (See Column 1 Lines 17-20 and Column 2 Lines 7-16). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kitamura to include mesas and diffusions that have RESURF as disclosed in Ranjan because it aids in controlling the breakdown voltage.

8. Claims 7 and 22-28 are rejected under 35 U.S.C. 103(a) as obvious over Kitamura et al. (U.S. Patent No. 5,844,275) in view of Ranjan (U.S. Patent No. 5,861,657), Sakakibara et al. (U.S. Patent No. 5,449,946) and Malhi (U.S. Patent No. 5,539,238).

In regards to claim 7, Kitamura fails to disclose the following:

a) insulation layer interposed between said substrate and said trench receiving layer the upper surface of said insulation layer being coplanar with the bottoms of said trenches.

However, Malhi discloses an insulating layer (See Column 3 Lines 13-18). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kitamura to include an insulating layer as disclosed in Malhi because it aids in keeping the devices from shortening out.

In regards to claim 22, Kitamura discloses the following:

a) a dielectric filler in each of said trenches (See Figure 1).

In regards to claims 23 and 25 Kitamura discloses the following:

a) source, drain and gate contacts supported on said upper surface and connected to said source region, gate electrode and drain regions respectively (See Figure 1).

In regards to claims 24 and 26-28 Kitamura discloses the following:

a) substrate is a lightly doped P type material (See Figure 1).

In regards to claims 24 and 26-28 Kitamura fails to disclose the following:

a) diffusion and said mesas have RESURF concentrations.

However, Ranjan discloses a semiconductor device where the mesas and diffusions have RESURF (See Column 1 Lines 17-20 and Column 2 Lines 7-16). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kitamura to include mesas and diffusions that have RESURF as disclosed in Ranjan because it aids in controlling the breakdown voltage.

Conclusion

7. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Coe (U.S. Patent No. 4,754,310) discloses a high voltage semiconductor device; b) Baliga (U.S. Patent No. 5,233,215) discloses a silicon carbide power mosfet; c) Baliga (U.S. Patent No. 5,323,040) discloses a silicon carbide field effect device; d)

Houston (U.S. Patent No. 5,436,173) discloses a method for forming a soi device; f) Floyd et al. (U.S. Patent No. 5,592,005) discloses a punch through field effect transistor; g) Ranjan (U.S. Patent No. 5,801,431) discloses a mos gated semiconductor device; h) Bhatnagar et al. (U.S. Patent No. 5,710,455) discloses a lateral mosfet with modified field plates; i) Martinelli (U.S. Patent No. 4,605,948) discloses a semiconductor structure for electric field distribution; j) Terashima et al. (U.S. Patent No. 5,874,767) discloses a semiconductor device including a lateral power device; k) Fujishima et al. (U.S. Patent No. 5,885,878) discloses a lateral trench mosfet; l) Uenishi et al. (U.S. Patent No. 6,040,600) discloses a trenched high breakdown voltage semiconductor device; and m) Funaki (U.S. Patent No. 6,069,396) discloses a high breakdown voltage device.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

July 23, 2002

Carl Whitehead Jr.

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